

PART NO.:

FOR MESSRS:

## CONTENTS

NO.	ITEM	PAGE
1.	COVER	1
2.	RECORD OF REVISION	2
3.	GENERAL SPECIFICATION AND MECHANICAL DATA	3
4.	ABSOLUTE MAXIMUM RATINGS	4
5.	ELECTRICAL CHARACTERISTICS	5
6.	OPTICAL CHARACTERISTICS	6
7.	BLOCK DIAGRAM	7
8.	TIMING CHARACTERISTICS	8
9.	DIMENSIONAL OUTLINE	9 ~ 11
10.	FUNCTIONAL DESCRIPTION	12 ~ 20

Accepted by: \_\_\_\_\_

Proposed by: Jack Hon 7/05  
195

# RECORD OF REVISION

DATE	PAGE	SUMMARY
5-10-'96	3	1) 3.3(2) MODULE SIZE: 35.7H → 34.7H 2) ICOM CONTROL LINE: Y20 → Y21.Y37 → Y32. Y38 → Y33.Y55 → Y58.Y69 → Y70.Y82 → Y79.
	7	
	9	3) PCB HEIGHT: 35.7 → 34.7mm 4) PIN NO. 3: RES → LEDB.L
	10	
7-05-'96	3	1) MODULE SIZE: 6.8D → 7.3D 2) 3.3(3)EFFECTIVE AREA: 44.5W → 43.7W 26.6W → 25.7H 3) 3.3(4) ACTIVE AREA: 39.96W → 38.97W, 21.56H → 20.13H. 4) DOT SIZE: 0.41H → 0.39H, 5) DOT PITCH: 0.40W → 0.39W, 0.45H → 0.42H. 6) LCD TYPE: G → Y
	4	7) 4.2 SHOCK: OPERATING 3G max → 10G max. STORAGE 50G max → 100G max.

### 3. GENERAL SPECIFICATIONS AND MECHANICAL DATA

#### 3.1 GENERAL SPECIFICATIONS

PLEASE REFER TO:

"CUSTOMER ACCEPTANCE STANDARD SPECIFICATONS (MS-10-10000)".

3.2 THIS INDIVIDUAL SPECIFICATON IS PRIOR TO GENERAL SPECIFICATIONS.

#### 3.3 MECHANICAL DATA

(1) NUMBER OF DOTS -----	100W * 48H DOTS
(2) MODULE SIZE -----	48.7W * 34.7H * 7.3D (max) mm
(3) EFFECTIVE AREA -----	43.7W * 25.7H mm
(4) ACTIVE AREA -----	38.97W * 20.13H mm
(5) DOT SIZE -----	0.36W * 0.39H mm
(6) DOT PITCH -----	0.39W * 0.42H mm
(7) VIEWING DIRECTION -----	6 O'CLOCK
(8) LCD TYPE -----	STN.YELLOW.TRANSFLECTIVE.
(9) LED COLOR -----	YELLOW-GREEN

#### 4. ABSOLUTE MAXIMUM RATINGS

##### 4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS.

I T E M	SYMBOL	MIN.	MAX.	UNIT	COMMENT
POWER SUPPLY FOR LOGIC	VDD-VSS	0	7.0	V	
INPUT VOLTAGE	VI	VSS	VDD	V	
STATIC ELECTRICITY	—	—	100	V	NOTE (1)
POWER SUPPLY FOR LED	VLED	—	6.0	V	

NOTE (1) : TEST METHOD AND CONDITIONS AFTER CHARGING UP 200 PF CAPACITOR BY STATED VOLTAGE. THE CAPACITOR IS CONNECTED WITH INTERFACE PINS OF THE MODULE.

##### 4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS.

I T E M	OPERATING		STORAGE		COMMENT
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	-20℃	70℃	-30℃	80℃	NOTE (2)
HUMIDITY	NOTE (3)		NOTE (3)		WITHOUT CONDENSATION
VIBRATION NOTE (4)	—	0.5G	—	2G	10~300HZ XYZ DIRECTIONS 1 Hr EACH
SHOCK NOTE (4)	—	10G	—	100G	10 μSEC XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (2) : Ta AT -30℃ : 48HR MAX.

80℃ : 168HR MAX.

NOTE (3) : Ta ≤ 60℃ : 85% RH MAX.

Ta > 60℃ : ABSOLUTE HUMIDITY MUST BE LOWER THAN THE

HUMIDITY OF 85% RH AT 50℃ . (50% RH AT 70℃)

NOTE (4) : 1G = 9.8 m /

## 5. ELECTRICAL CHARACTERISTICS.

I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
POWER SUPPLY VOLTAGE FOR CIRCUIT	VDD-VSS	—————	4.75	5.0	5.25	V
INPUT VOLTAGE NOTE (2)	VIH	H LEVEL	2.0	———	VDD	V
	VIL	L LEVEL	0	———	0.8	V
OUTPUT VOLTAGE NOTE (1)	VOH	IOH = -0.3mA	2.4	———	—	V
	VOL	IOL = 3.0mA	———	———	0.4	V
POWER SUPPLY CURRENT NOTE (3)	IDD	VDD-VSS=5.0V	———	3.0	5.0	mA
LCD DISPLAY DUTY RATIO	DUTY	—————	———	1/65	—	—
POWER SUPPLY CURRENT FOR LED	ILED	VLED(+) = 5.0V	———	40	45	mA

NOTE (1) : APPLIED TO TERMINALS D0 ~ D7

NOTE (2) : APPLIED TO TERMINALS E , A0 , D0 ~ D7 , R/W

NOTE (3) : THE DISPLAY PATTERN IS ALL "ON" , OR ALL "OFF"

NOTE (4) : RECOMMENDED LCD DIRVING VOLTGE MAY FLUCTUATE ABOUT  
= 0.5V BY EACH MODULE.

## 6. OPTICAL CHARACTERISTICS

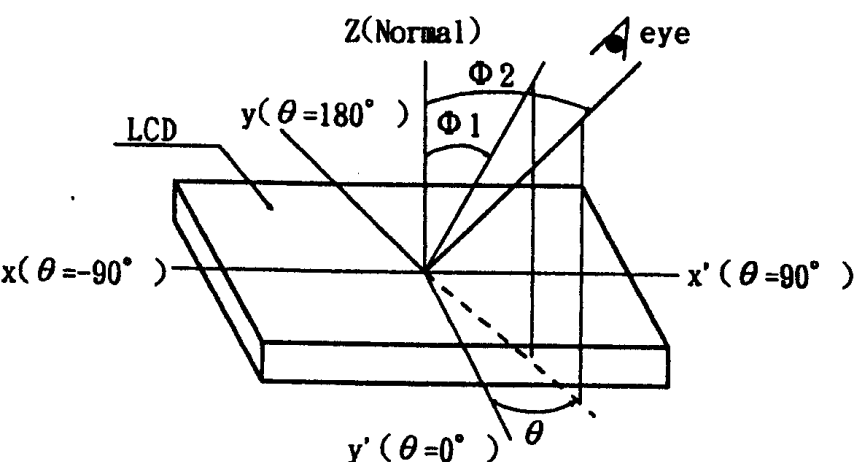
$T_a = 25^\circ\text{C}$

I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
VIEWING AREA	$\Phi 2 - \Phi 1$	$K = 1.4$	30	40	—	deg.	1~3
CONTRAST RATIO	K	$\Phi = 10^\circ$ $\theta = 0^\circ$	3.0	5.0	—	—	1~3
RESPONSE TIME	tr(rise)	$\Phi = 10^\circ$ $\theta = 0^\circ$	—	250	—	ms	1, 4
	tf(fall)	$\Phi = 10^\circ$ $\theta = 0^\circ$	—	350	—	ms	1, 4
THE BRIGHTNESS OF BACKLIGHTING SOURCE	B	( * ) $\Phi = 0^\circ$ $\theta = 0^\circ$	3.0	—	—	cd/m <sup>2</sup>	—

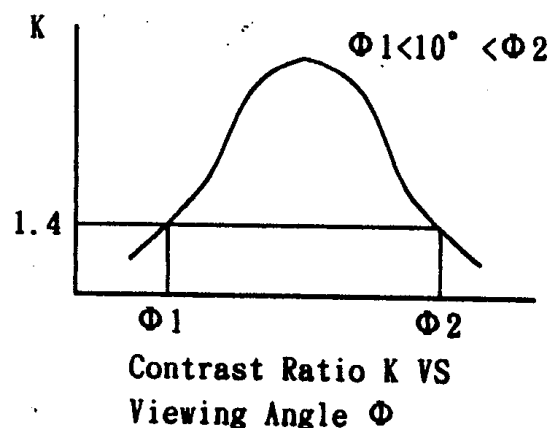
( \* UNDER NORMAL TEMPERATURE AND HUMIDITY IN A DARK ROOM )

NOTE (1) : SEE CUSTOMER ACCEPTANCE STANDARD SPECIFICATION FOR DEFINITION OF OPTICAL CHARACTERISTICS

NOTE 1. DEFINITION OF ANGLE  $\theta$  AND  $\Phi$

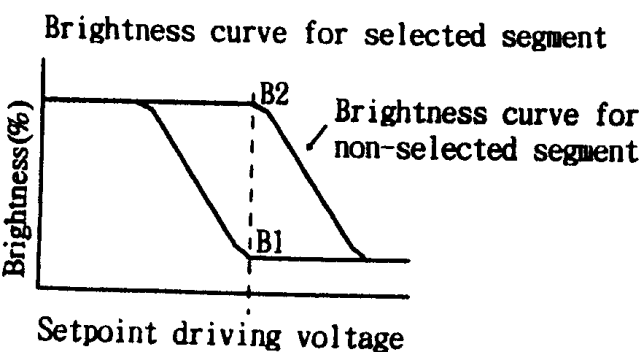


NOTE 2. DEFINITION OF VIEWING ANGLE  $\Phi 1$  AND  $\Phi 2$

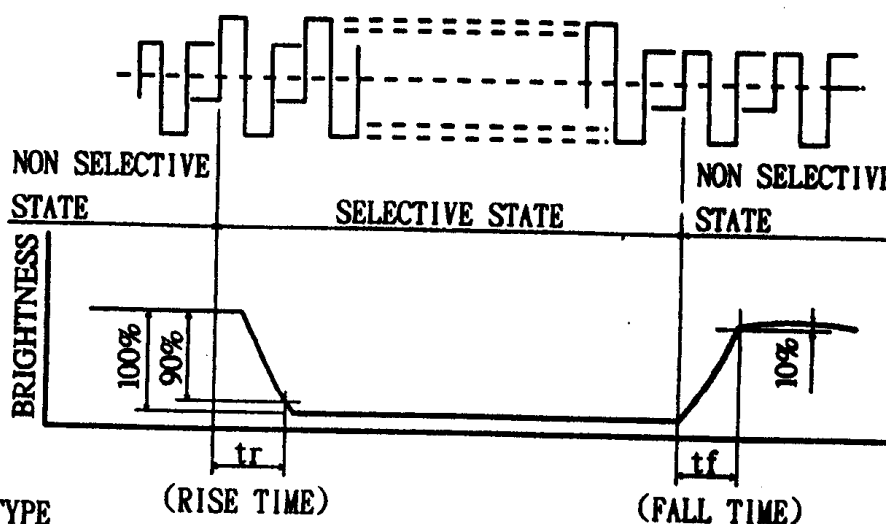


NOTE 3. DEFINITION OF CONTRAST "K"

$$K = \frac{\text{Brightness of non-selected segment}(B2)}{\text{Brightness of selected segment}(B1)}$$



NOTE 4. DEFINITION OF OPTICAL RESPONSE

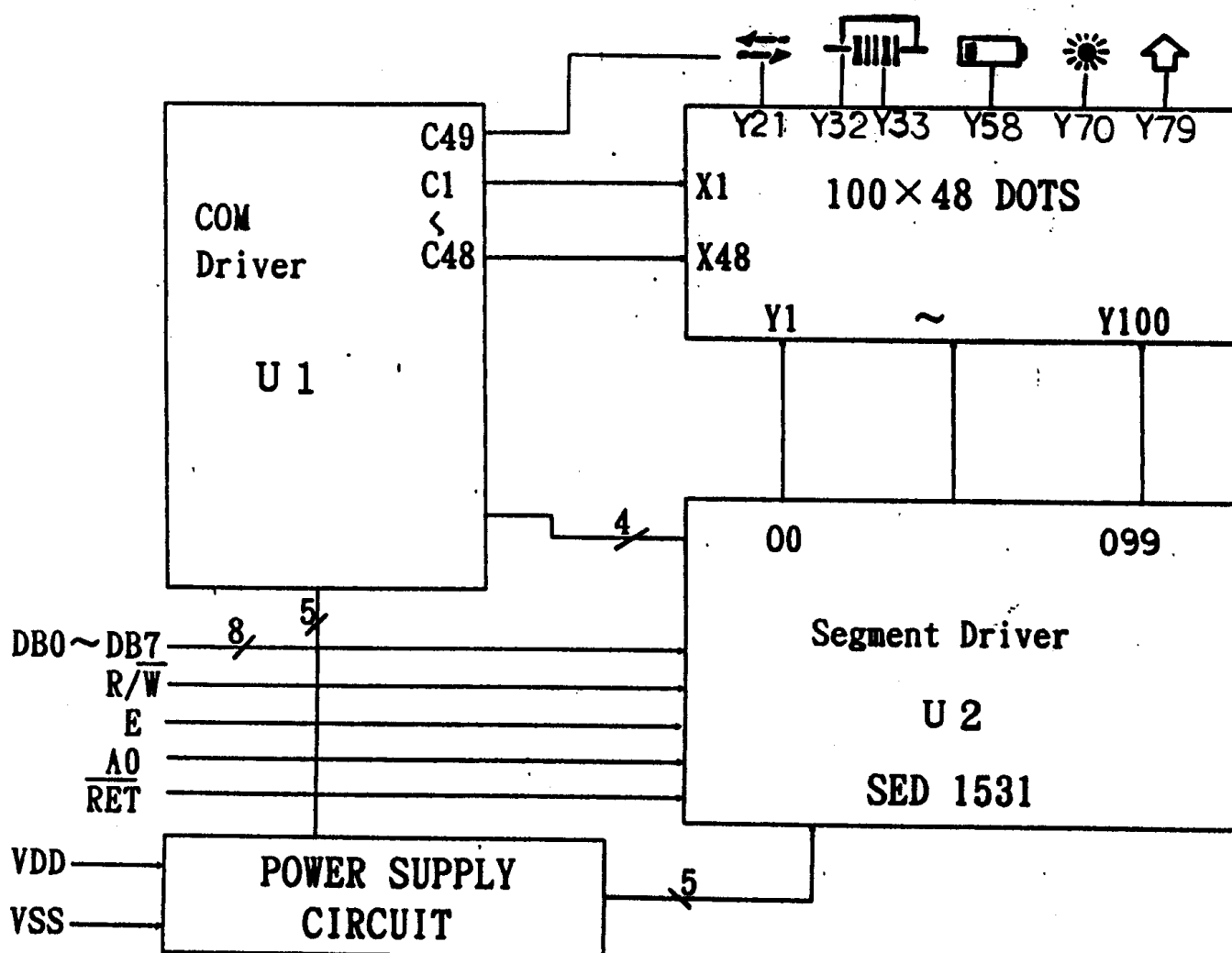


POSITIVE TYPE

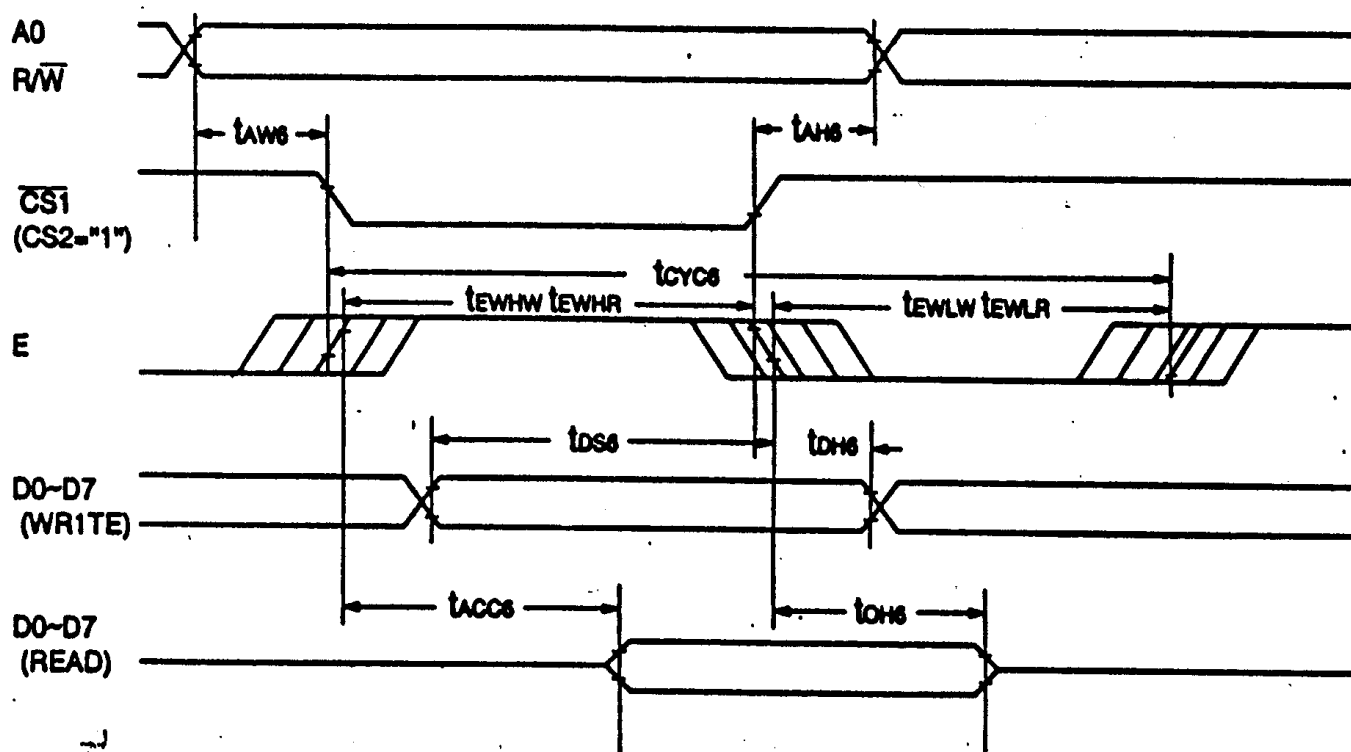
(RISE TIME)

(FALL TIME)

## 7. BLOCK DIAGRAM



## 6. TIMING CHARACTERISTICS



$V_{DD} = 5.0 V \pm 10\%$ ,  $T_a = -40$  to  $+85^\circ C$

V<sub>DD</sub> = 5.0 V ±10%, T<sub>A</sub> = -40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t <sub>CYCS</sub>		166	—	ns
Address setup time		A0 W/R	t <sub>AWs</sub>		10	—	ns
Address hold time			t <sub>AHs</sub>		10	—	ns
Data setup time		D0 to D7	t <sub>DsS</sub>		20	—	ns
Data hold time			t <sub>DHs</sub>		10	—	ns
Output disable time			t <sub>OHs</sub>	CL=100pF	10	50	ns
Access time			t <sub>ACCS</sub>		—	70	ns
Enable	READ	E	t <sub>EWHR</sub>		70	—	ns
low pulse width	WRITE		t <sub>EWHW</sub>		30	—	ns
Enable	READ	E	t <sub>EWLR</sub>		70	—	ns
high pulse width	WRITE		t <sub>EWLW</sub>		100	—	ns



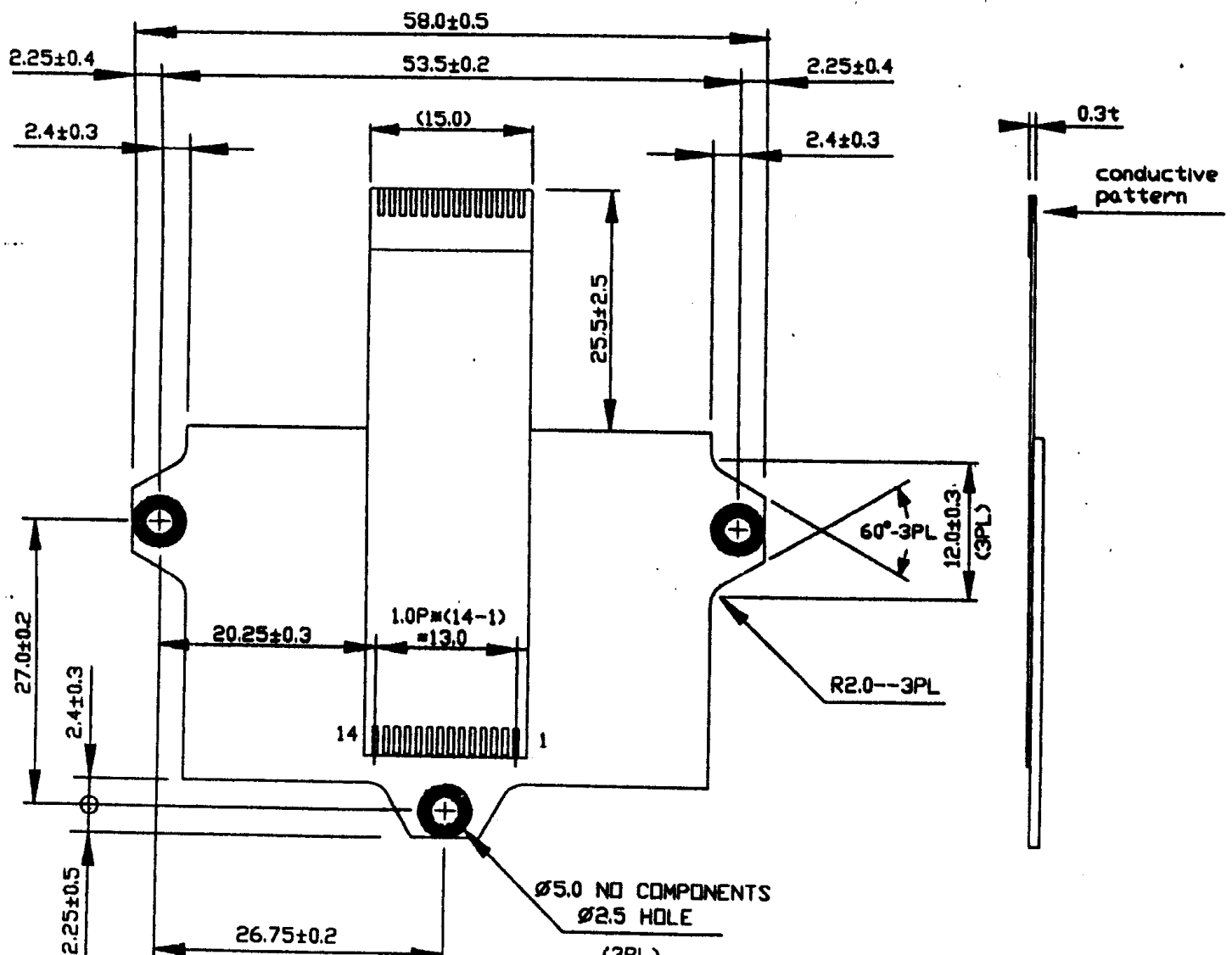
Technical drawing of a DOT matrix module, showing top and side views with dimensions.

**Top View Dimensions:**

- Overall width:  $48.7 \pm 0.3$
- Overall height:  $34.7 \pm 0.3$
- Top edge dimensions (from left):  $2.4 \pm 0.3$ ,  $6.4 \pm 0.3$ ,  $3.9 \pm 0.2$
- Left edge dimensions (from top):  $33.7 \pm 0.3$ ,  $25.7 \pm 0.3$ ,  $20.13 \pm 0.1$
- Internal vertical dimensions:  $2.1$ ,  $1.0 \pm 0.2$
- Top edge dimensions (from right):  $4.9 \pm 0.3$  (2.365),  $43.7 \pm 0.3$ ,  $38.97 \pm 0.1$ ,  $6.85 \pm 0.2$ ,  $30.0 \pm 0.1$
- Central area labels: "ICDN AREA", "DOT MATRIX", "DOT SIZE  $0.36 \times 0.39$ ", "DOT PITCH  $0.39 \times 0.42$ "

**Side View Dimensions:**

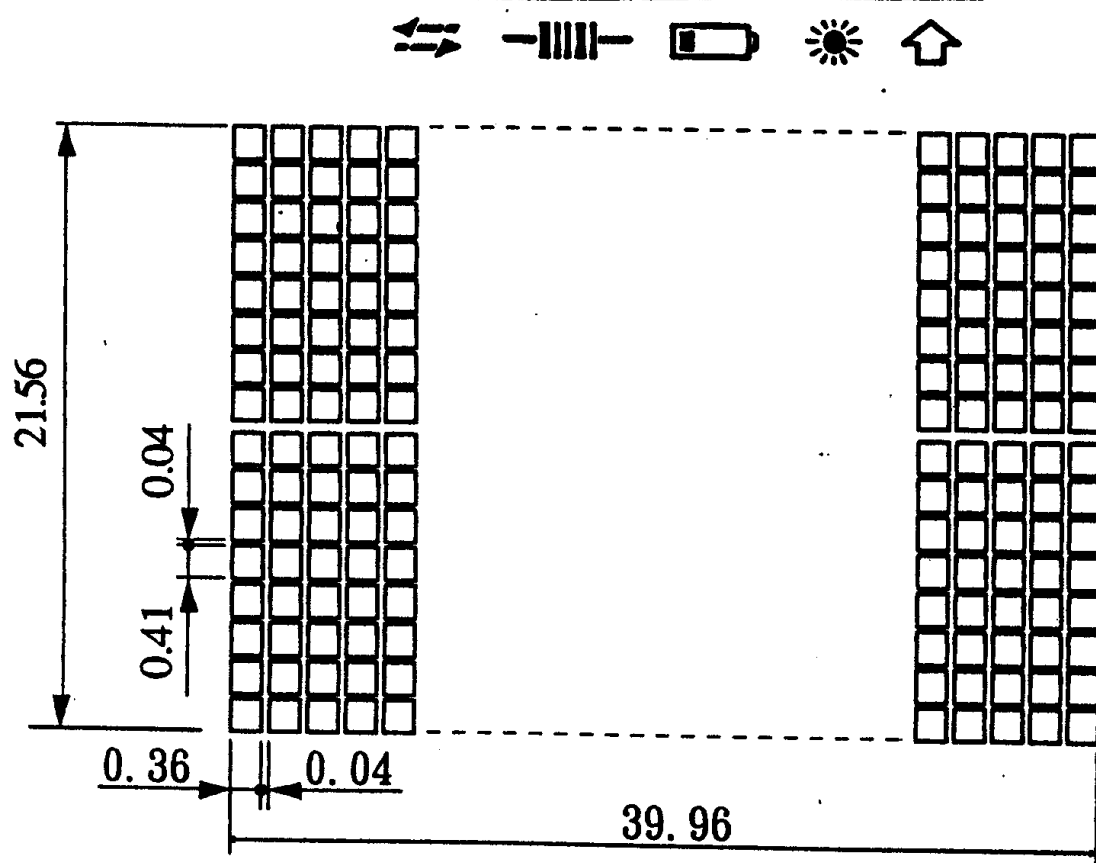
- Top edge dimension:  $7.3 \text{ max}$
- Bottom edge dimension:  $1.0 \text{ t}$
- Overall height:  $4.8 \pm 0.3$



## 9.2 INTERFACE

PIN NO.	SYMBOL	LEVEL	FUNCTION
1	VSS	GND	GROUND
2	VDD	5.0V	POWER SUPPLY FOR LOGIC
3	$\overline{\text{IEDB.L}}$	GND	GROUND:LED ON
4	A0	L/H	A0="L" INSTRUCTION REGISTER A0="H" DATA REGISTER
5	R/ $\overline{\text{W}}$	L/H	H:DATA READ (LCD MODULE $\rightarrow$ MPU ) L:DATA WRITE (LCD MODULE $\leftarrow$ MPU )
6	E	—	ENABLE SINGAL
7	DB7	—	DATA INPUT/OUTPUT (MSB)
8	DB6	—	DATA INPUT/OUTPUT
9	DB5	—	DATA INPUT/OUTPUT
10	DB4	—	DATA INPUT/OUTPUT
11	DB3	—	DATA INPUT/OUTPUT
12	DB2	—	DATA INPUT/OUTPUT
13	DB1	—	DATA INPUT/OUTPUT
14	DB0	—	DATA INPUT/OUTPUT (LSB)

### 9.3 DETIL DRAWING OF MATERIX PATTERN AND ICOM



# 10. FUNCTIONAL DESCRIPTION

Command	Code											Function
	A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns on LCD panel when goes high, and turns off when goes low.
(2) Initial Display Line	0	1	0	0	1	Start display address					Specifies RAM display line for COM0.	
(3) Set Page Address	0	1	0	1	0	1	1	Page address			Sets the display RAM page in Page Address register.	
(4) Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address			Sets 4 higher bits of column address of display RAM in register	
(4) Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address			Sets 4 lower bits of column address of display RAM in register	
(5) Read Status	0	0	1	Status				0	0	0	0	Reads the status information.
(6) Write Display Data	1	1	0	Write data							Writes data in display RAM.	
(7) Read Display Data	1	0	1	Read data							Reads data from display RAM.	
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when high.
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	Normal indication when low, but full indication when high.
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1).
(11) Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0 1	Sets LCD drive voltage bias ratio.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Power Control	0	1	0	0	0	1	0	1	Operation status		Selects the power circuit operation mode.	
(16) Set Electronic Control Register	0	1	0	1	0	0	Electronic control value				Sets V5 output voltage to Electronic Control register.	
(17) Set Standby	0	1	0	1	0	1	0	1	1	0	0 1	Selects standby status. 0: OFF 1: ON
(18) Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON

## Command set

### (1) Display ON/OFF

Alternately turns the display on and off.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

The display turns off when D goes low, and it turns on when D goes high.

### (2) Start Display Line

Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. THE RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						⋮
1	1	1	1	1	0	62
1	1	1	1	1	1	63

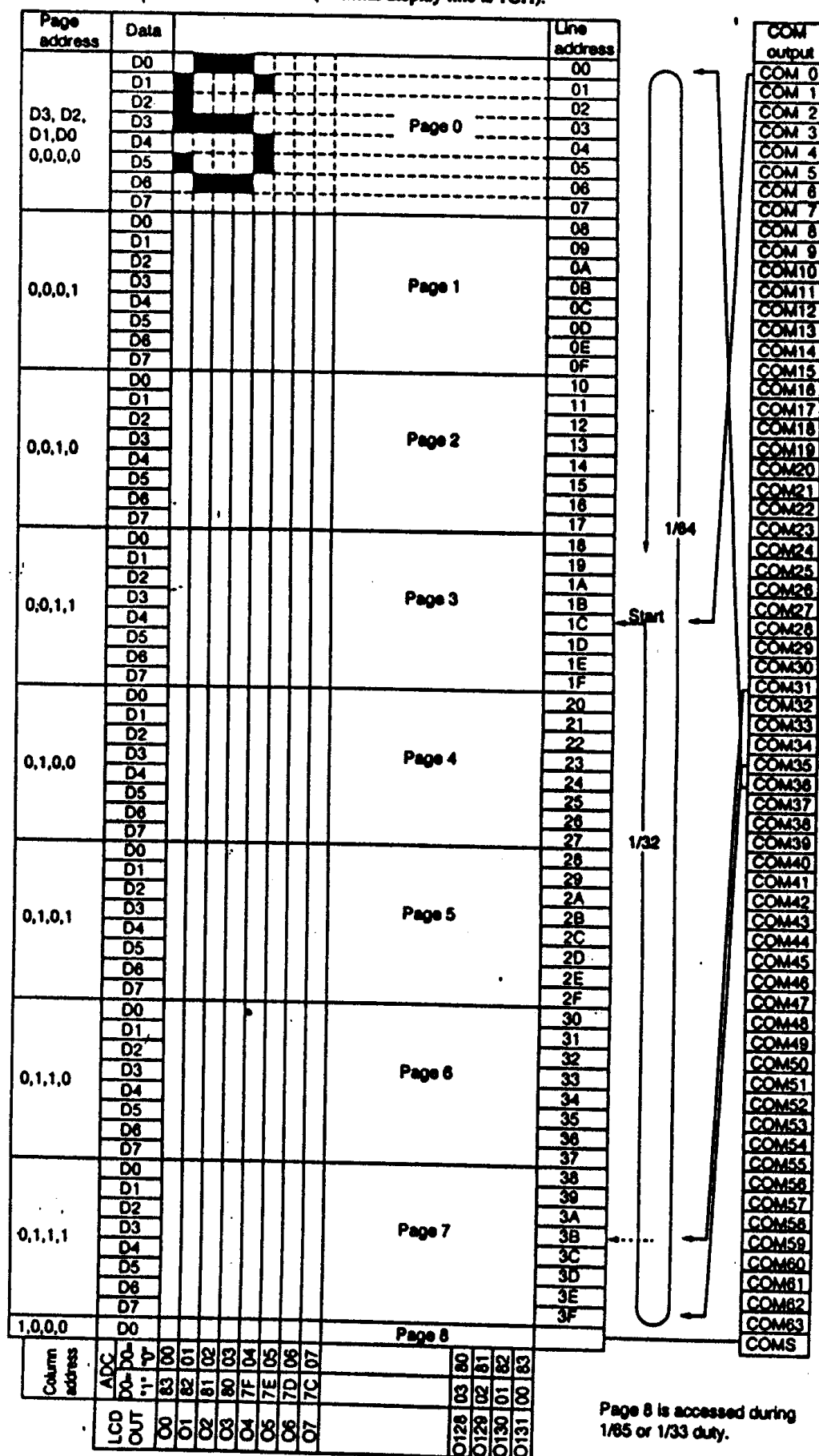
### (3) Set Page Address

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicated to the indicator, and only D0 is valid for data change.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

# 10. FUNCTIONAL DESCRIPTION

Relationship between display data RAM and addresses (if initial display line is 1CH):



A3	A2	A1	A0	Page Address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

#### (4) Set Column Address

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access to the display RAM, the column address counter is incremented by 1 during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lorer bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
1	0	0	0	0	0	1	1	131

#### (5) Read Status

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

**BUSY:** When high, the LCM is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

**ADC:** Indicates the relationship between RAM column address and segment drivers. When low, the display is normal and column address "131-n" corresponds to segment driver n. When high, the display is reversed and column address n corresponds to segment driver n.

**ON/OFF:** Indicates whether the display is on or off. When goes low, the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

**RESET:** Indicates the initialization is progress by RES signal or by Reset command. When low, the display is on. When high, the LCM is being reset.

(6) Write Display Data

Writes 8-bit data in display RAM. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each read, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pins can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction). When D is high, the left rotation (reverse direction).  
Fig.5 shows the status.

LCD output		000000001								
ADC (D0)	"0" "1"	0(H) → COLUMN ADDRESS → 83(H) 83(H) ← ← 0(H)								

(9) Normal/reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display).

When D is high, the RAM data is low, being LCD ON potential (reverse display).



(10) Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

(11) Set LCD Bias

Selects a bias ratio of the voltage required for driving the LCD. This command is enabled when the voltage follower in the power supply circuit operates.

A	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

D	Bias ratio of LCD power supply
0	1/8 bias
1	1/6 bias

(12) Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremented by Read Display Data command but incremented by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write.

(13)End

Cancels Read-Modify-Write mode and returns counn address to the original address(when Read-Modify-Write was issued).

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

(14)Reset

Resets the Initial Display Line register,Column Address counter,Page Address register,and output status selector circuit to their initial status.The Reset command does not affect on the contents of display RAM.Refer to the Reset circuit section of FUNCTIONAL DESCRIPTION.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply.Only the Reset siganl to the RES pin can initialize supplies.

(15)Set Power Control

Selects one of eight power circuit functions using 3-bit register.An extemal power supply and part of intemal power supply functions can be used simultaneously.Refer to Power Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 goes low,voltage follower turns off.When A0 goes high it turns on.

When A1 goes low,voltage regulator turns off.When A1 goes high it tuons on.

When A2 goes low,voltage booster turns off.When A2 goes high it turns on.

(16)Set Electronic Control

Adjusts the contrast of LCD panel display by changing V5 LCD drive voltage that is output by voltage regulator of on-board power supply.

This command selects one of 32 LCD drive voltages by storing data in 5-bit register.The voltage adjusing range should be determined depending on the extemal resistance.Refer to the V-voltage Regulator Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	A4	A3	A2	A1	A0

D4	D3	D2	D1	D0	Driving Voltage
0	0	0	0	0	Low
0	0	0	0	1	
0	0	0	1	0	
					↓
1	1	1	0	1	High
1	1	1	1	0	
1	1	1	1	1	

Set register to (D4,D3,D2,D1,D0)=(0,0,0,0,0) to suppress electronic control function.

#### (17) Static Indicator

This command turns on or off static drive indicators. The indicators display is controlled by this command only, and it is not affected by the other display control commands. Either FR or FRS terminal is connected to either of static indicator LCD drive electrodes, and the remaining terminal is connected to another electrode. When the indicator is turned on the static drive operates and the indicator blinks at an interval of approximately one second. The pattern separation between indicator electrodes and dynamic drive electrodes is recommended. A closer pattern may cause an LCD and electrode deterioration.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

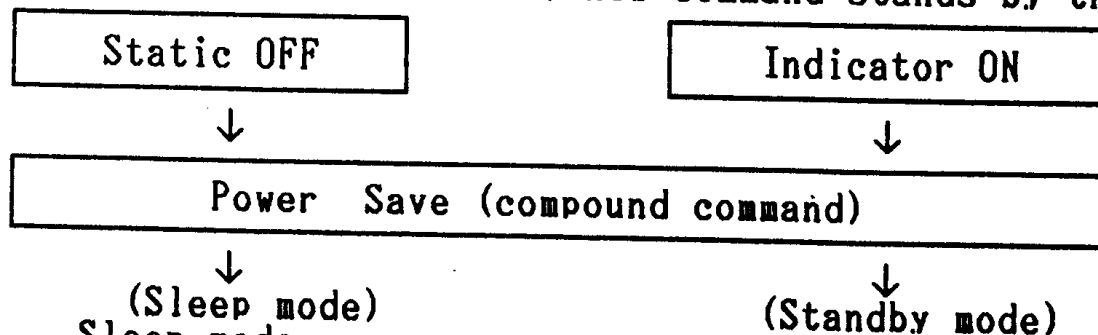
D 0: Static indicator OFF

1: Static indicator ON

#### (18) Power Save (Compound Command)

When all displays are turned on during indicator off, the Power Save command is issued to greatly reduce the current consumption.

If the static indicators are off, the Power Save command sleeps the system. If on, this command stands by the system.



Sleep mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

- (1) Stops the oscillator circuit and LCD power supply circuit.
- (2) Stops the LCD drive and outputs the VDD level as the segment/common driver output.

(3) Holds the display data and operation mode provided before the start of the sleep mode.

(4) The MPU can access to the built-in display RAM.

#### Standby mode

Stops the operation of the duty LCD display system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive.

The ON operation of the static drive system indicates that the LCM is in the standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.

(2) Stops the LCD drive and outputs the VDD level as the segment/common driver output. However, the internal static drive system operates.

(3) Holds the display data and operation mode provided before the start of the standby mode.

(4) The MPU can access to the built-in display RAM.

When the RESET command is issued in the standby mode, the sleep mode is set.

When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VDD level, prior to or concurrently with causing the LCM to go to the sleep mode or standby mode.

When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VDD level, prior to or concurrently with causing the LCM to go to the sleep mode or standby mode.